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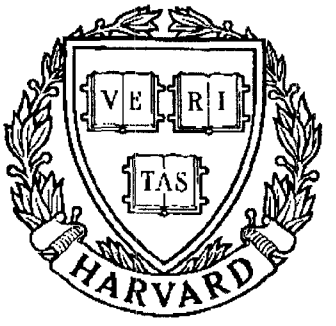

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Area-Efficient Switched Capacitor Non-Filtering Circuits: Sum-Gain Amplifiers

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Area-Efficient Switched Capacitor Non-Filtering Circuits: Sum-Gain Amplifiers

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Abstract

Switched-capacitor sum-gain amplifiers (SGAs) are widely used in parallel filter systems. The capacitance spread of such circuits is proportional to the coefficient spread, thus making conventional SGAs un-suitable for high gain applications. SGAs with different input phases and a SGA with the same input phase are discussed, and a new area-efficient SGA, which can reduce the capacitance spread to the square root of coefficient spread ratio, is proposed. Furthermore, the non-ideal effects of op-amp like finite DC gain and offset voltage are compensated by using the offset storing capacitor. All the circuits designed here only use the bi-phase clocking scheme.

1 Introduction

One of important switched capacitor non-filtering circuits is the sum-gain amplifier (SGA) which can do addition and subtraction at the same time. The basic circuit structure of the SGA circuit is shown in Fig. 1. As pointed out

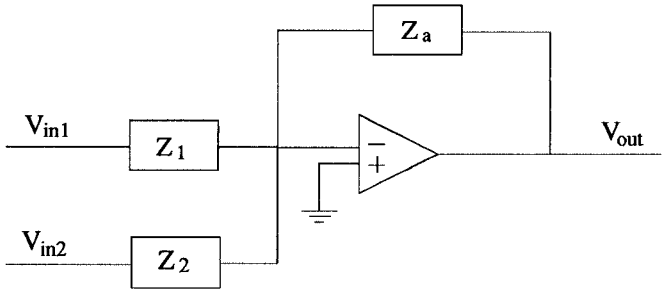

Figure 1: Sum-gain amplifier circuit.

in [1], there are several ways to implement the impedance Z. The simpliest way is to choose all impedances Z_i as the un-switched capacitors. However, the inverting input terminal of op-amp is floating in such an arrangement and even a small leakage current will saturate the op-amp. Besides, only the subtraction of input voltages is allowed in such a scheme. The other way to build the impedance is to use the switched capacitors. Even this kind of arrangement can solve the current leakage problem and can do the addition and subtraction at the same time, but the op-amp is open-circuited in half period.

Therefore, the op-amp may easily drift to the saturation. From the above discussion, it seems to be reasonable to use the un-switched and switched capacitors in parallel. However, the complexity of entire circuits will become much higher and the output offset voltage is also increased. Thus, the other suitable circuit topologies should be pursued.

2 SGA with Different Input Phases

To reduce the circuit complexity and the effects of op-amp offset voltage, the compensated circuit was designed by [1] and shown in Fig. 2. Assume

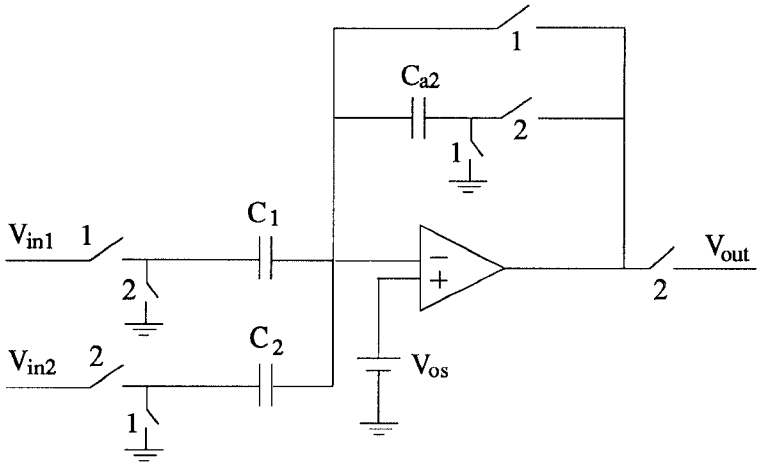

Figure 2: Gregorian's sum-gain amplifier circuit.

$V_{in2} = 0$ and the DC gain of op-amp is ∞, when the switches 1 are closed, the

op-amp performs as a unity-gain follower, with the voltage of V_{os}. Therefore, the capacitor C_1 is charged to $V_{in1} - V_{os}$ and the capacitor C_{a2} is charged to V_{os}. When the switches 2 are closed, C_1 is discharged to $-V_{os}$, while C_{a2} becomes $V_{os} - V_{out}(n + 1/2)$. From the charge conservation,

$$C_1[-V_{os} - (V_{in1} - V_{os})] = C_{a2}[(V_{os} - V_{out}(n + \frac{1}{2})) - V_{os}] \tag{1}$$

is satisfied. Hence, the V_{os} is cancelled and results in

$$V_{out}(n + \frac{1}{2}) = \frac{C_1}{C_{a2}} V_{in1}(n). \tag{2}$$

By choosing the appropriate capacitor values of C_1 and C_{a2}, the non-inverting gain can be achieved easily. On the other hand, if the V_{in1} is assumed to be zero and the V_{in2} is used, the inverting voltage amplifier can be obtained. Combining the V_{in1} and V_{in2} together, this sum-gain-amplifier can do addition and subtraction simultaneously.

The operational principle of this SGA can be stated as follows. Every capacitor plate which is connected to the inverting terminal of op-amp can not be disconnected any time. Therefore, the offset voltage can be cancelled in the consecutive phase. This kind of circuits is stray-insensitive but high-slew rate op-amp is needed to reset op-amp output in one phase. Note that the input phases are different in the addition and subtraction.

To avoid the use of the high-speed op-amps, an improved SGA shown in Fig. 3 was proposed by [2]. This is due to the observation that the op-

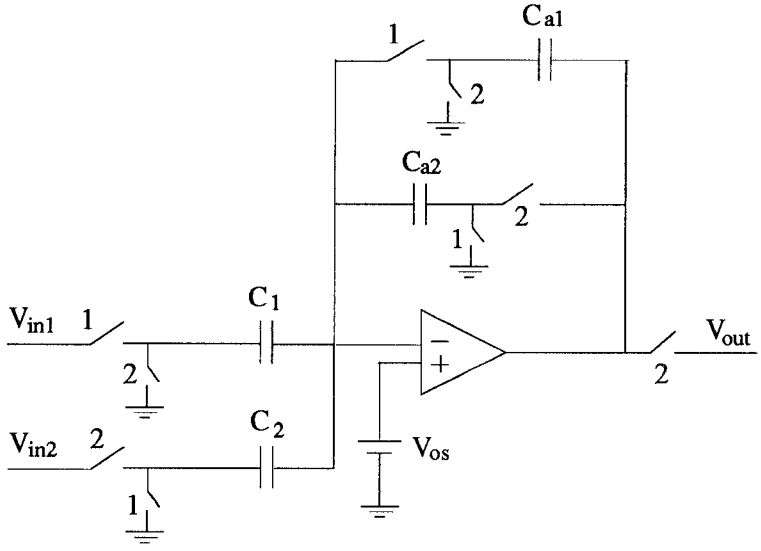

Figure 3: Haug's sum-gain amplifier circuit.

amp functions like a unity-gain amplifier during one phase, therefore the response of op-amp has to be fast enough to reset the output voltage. If one additional capacitor C_{a1} is used to store this charge, the high-slew rate op-amp can be avoided. Assume input $V_{in1} = 0$ and the DC gain of op-amp is ∞, the functions of the capacitors of C_2 and C_{a2} are the same as the above discussions. The difference is to use the capacitor C_{a1} and its associated switches instead of using only one switch. During the period of phase 2, the

voltage of the capacitor C_{a1} is charged to $-V_{out}(n-1/2)$. In the phase 1, the charge stored in the capacitor C_{a2} is pulled back and eliminated by the capacitor C_2, but the LHS plate of the capacitor C_{a1} is connected to the inverting terminal of op-amp. The output voltage is not reset but becomes $V_{os} - V_{out}(n-1/2)$, thus only the change of V_{os} which may be only few mV instead of resetting the output voltage which may be couple V is needed. In this case, no high slew-rate op-amp is required. From time domain analysis, the following equations can be obtained.

$$V_{out}(n-\frac{1}{2}) = -\frac{C_2}{C_{a2}}V_{in2}(n-\frac{1}{2}) \tag{3}$$

$$V_{out}(n) = -\frac{C_2}{C_{a2}}V_{in2}(n-\frac{1}{2}) + V_{os} \tag{4}$$

The same analysis can be done for assuming $V_{in2} = 0$, and the following equations can be got.

$$V_{out}(n) = \frac{C_1}{C_{a2}}V_{in1}(n-1) + \frac{C_1}{C_{a1}}[V_{in1}(n-1) - V_{in1}(n)] + V_{os} \tag{5}$$

$$V_{out}(n+\frac{1}{2}) = \frac{C_1}{C_{a2}}V_{in1}(n) \tag{6}$$

Since the input signal is changed slowly, only the low slew-rate op-amp is needed. This kind of SGA is stray-insensitive and suitable for the application when the input phases are different for the addition and subtraction.

3 SGA with Same Input Phase

In some applications, the output signals are available only at the same time, therefore a SGA which can add and subtract the input signals in the same phase has to be designed. In this case, no sampled-and-held circuits are required before the input terminals of the SGA. A new sum-gain amplifier with same input phase [3] is shown in Fig. 4 and its principle of operation is as follows: Assume the op-amp is ideal here. Consider input V_{in1} first,

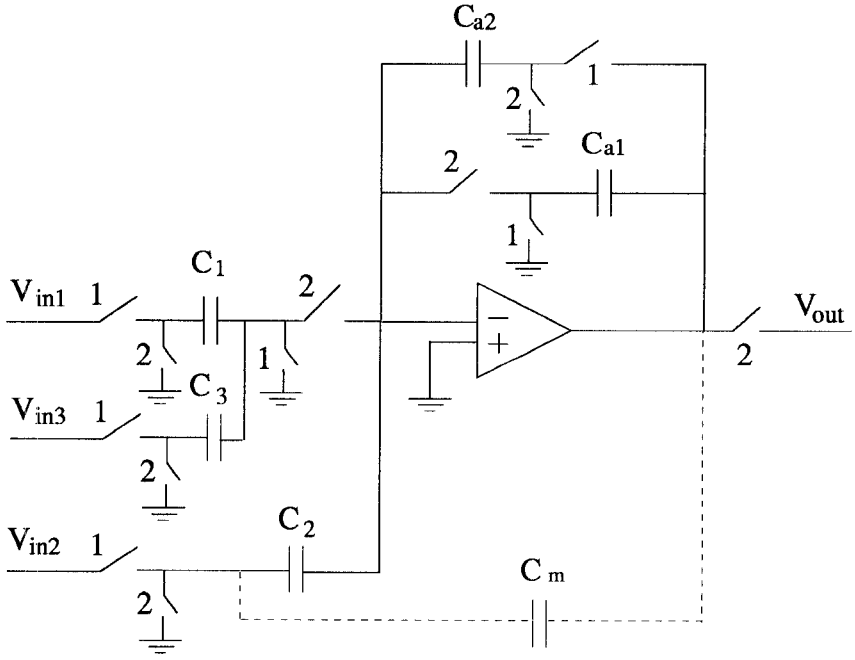

Figure 4: Sum-gain amplifier circuit with same input phase.

while V_{in2} and V_{in3} are set to zero. In phase 2, C_{a2} is discharged, and since in phase 1, its left plate is connected to the inverting terminal of the op-amp only, no charge can be injected to C_{a2}, and the output remains at ground level, which helps C_{a1} to discharge in this phase. During phase 2, C_1, C_{a1}, and the op-amp constitute a non-inverting gain stage, which gives $V_{out}(n+1/2) = (C_1/C_{a1})V_{in1}(n)$. The input V_{in3} can be analyzed in similar fashion.

Next, set V_{in1} and V_{in3} to zero. In phase 2, C_{a2} is discharged as in the previous case, but in phase 1, C_2, C_{a2}, and the op-amp constitute an inverting amplifier, hence, $V_{out}(n) = -(C_2/C_{a2})V_{in2}(n)$. This voltage is stored in C_{a1}, and is to be held constant during the next phase 2.

The final output is the superposition when all the 3 inputs are activated. The signal flow graph of the sum-gain amplifier is shown in Fig. 5, and the output voltage can be obtained as,

$$V_{out}(z) = (\frac{C_1}{C_{a1}}V_{in1}(z) - \frac{C_2}{C_{a2}}V_{in2}(z) + \frac{C_3}{C_{a1}}V_{in3}(z))z^{-1/2} \tag{7}$$

Hence, the output is the sum of V_{in1} and V_{in3}, while subtracts V_{in2}, all of which are scaled by appropriate gain factors. The gain factors can be individually controlled through C_1, C_2, and C_3. Moreover, it is obvious that this sum-

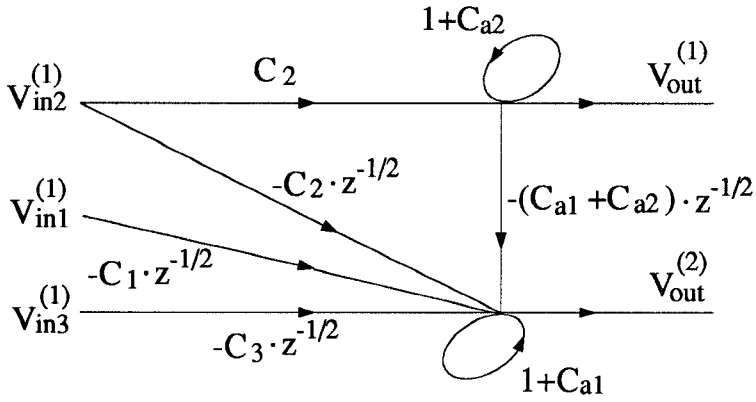

Figure 5: SFG of sum-gain amplifier circuit with same input phase.

gain amplifier can be designed to include any number of inputs for either addition or subtraction. It is noted that when assuming the offset voltage of op-amp is V_{os}, the DC gain is ∞, and setting V_{in1} and V_{in3} to be zero, this circuit functions like Fig. 3 does except the switching phases are different. The output voltage becomes

$$V_{out}(n-\frac{1}{2}) = -\frac{C_2}{C_{a2}}V_{in}(n-\frac{1}{2}) + V_{os} \tag{8}$$

Therefore, this circuit will be affected by the offset voltage of op-amp. Besides, when setting V_{in2} to be zero, the capacitor C_{a2} resets the output voltage to zero during the switches 1 are closed. Thus, the high slew-rate op-amp is required in this circuit.

One common disadvantage of all above sum-gain amplifiers is the lack of

a continuous feedback path across the op-amp. Hence, if the op-amp used in this circuit is very fast, a glitch at the output may occur at the non-overlapping interval between the two clock phases. Although it has been pointed out that such a glitch is harmless to the circuit performance[2, 4], this glitch can be easily removed by connecting a capacitor C_m between the op-amp output and the left plate of C_2[5, 3].

4 Area-efficient SGA

For the sum-gain amplifiers which are discussed so far, the capacitance spread ratio is proportional to the gain. This ratio is irrelevant to the sampling frequency. In the high-gain application, it is inevitable that large spread ratio is required, in the other words, large silicon area is needed. To overcome such a problem, the other circuit topologies have to be pursued.

The area-efficient sum-gain amplifiers which are proposed here use two steps to amplify the input signal. The spread ratio can be reduced to be approximately the square root of the gain, therefore a lot of area can be saved. An area-efficient SGA is designed and shown in Fig. 6. Assume the op-amp is ideal, and input voltages V_{in2} and V_{in3} are zero. When the switches

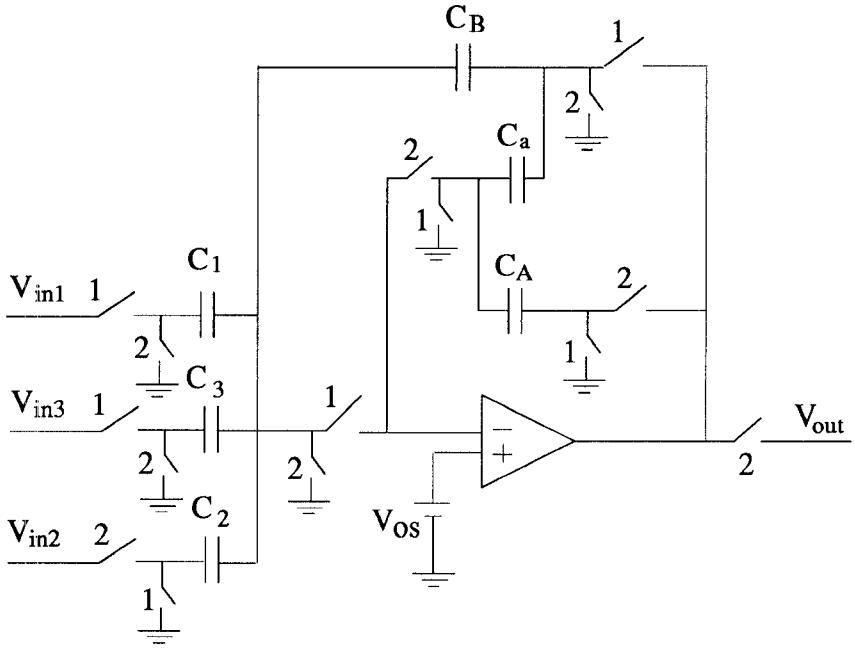

Figure 6: Area-efficient SGA circuit.

1 are closed, the input signal is amplified by the ratio of $-C_1/C_B$. At the same time, this voltage is sampled by the capacitor C_a. During the period 2, the switches 2 are closed. the voltage stored in C_a is amplified again by the ratio of C_a/C_A. The entire amplification is achieved by two capacitor ratios not a single one. Therefore, the capacitance spread ratio is much reduced. For the input voltages V_{in2} and V_{in3}, the same analysis can be derived. From

the signal flow graph, the output voltage can be easily obtained as

$$V_{out}(z) = \frac{-C_1 C_a V_{in1} z^{-1/2} - C_3 C_a V_{in3} z^{-1/2} + C_2 C_a V_{in2} z^{-1}}{C_A C_B}. \quad (9)$$

From the above result, again, this kind of circuit can be used as a sum-gain amplifier, that is, it does addition and subtraction simultaneously without changing circuit topology[6].

One thing has to be considered is the dynamic range of the amplifier. Due to the non-ideal effects of op-amps like offset voltages, the SGA may only have very small dynamic range. Assume the DC gain is ∞, offset voltage is V_{os}, and input voltages V_{in2} and V_{in3} are zero. When the switches 1 are closed,

$$V_{out}(n) = -\frac{C_1}{C_B} V_{in1}(n) + (1 + \frac{C_1}{C_B}) V_{os} \quad (10)$$

can be obtained. During the period 2, the following equation

$$V_{out}(n + \frac{1}{2}) = \frac{C_a}{C_A} V_{out}(n) + (1 + \frac{C_a}{C_A}) V_{os} \quad (11)$$

is satisfied. Combining the above two equations together, we can get

$$V_{out}(n + \frac{1}{2}) = -\frac{C_1 C_a}{C_A C_B} V_{in1}(n) + (1 + \frac{2C_a}{C_A} + \frac{C_1 C_a}{C_A C_B}) V_{os}. \quad (12)$$

For the high-gain amplification, the capacitor values of C_1 and C_a are much larger than those of capacitors C_A and C_B. It is obvious that the offset

voltage V_{os} is approximately amplified by the same factor of input voltage. Thus, the dynamic range is much reduced in such a design.

5 Area-efficient GOC SGA

To improve the dynamic range, a new area-efficient GOC SGA has been proposed. The circuit is shown in Fig. 7. The offset-storage capacitor C_o

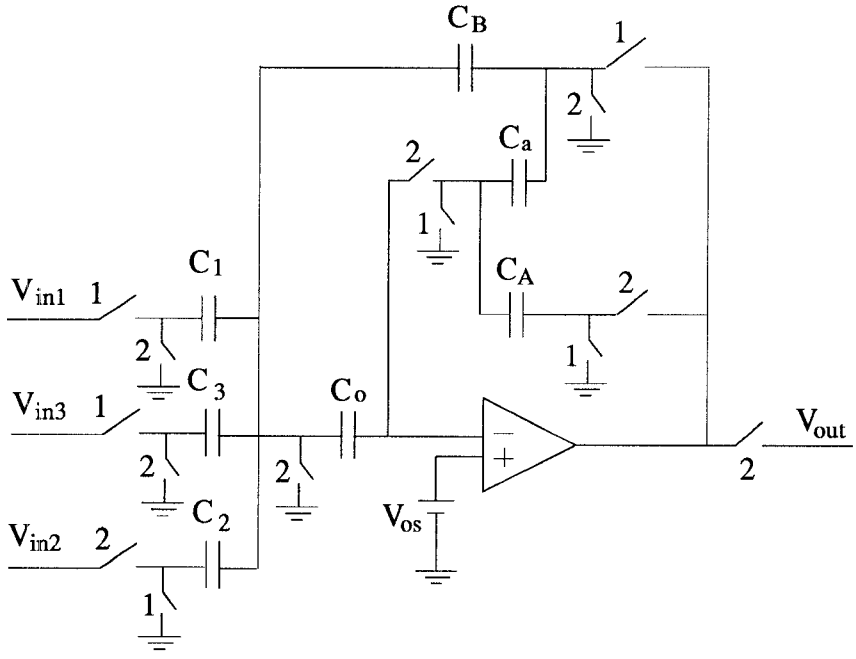

Figure 7: Area-efficient GOC SGA circuit.

is used in this circuit. Again, assume the DC gain is ∞, offset voltage is

V_{os}, and input voltages V_{in2} and V_{in3} are zero. When the switches 1 are closed, the junction among C_1, C_B, and C_o functions like the virtual ground because C_o has been charged to $-V_{os}$ in the previous phase and this voltage is preserved in this phase. Thus, the ideal charge transfer can be achieved. C_1 is the input capacitor and C_B is the integrating capacitor, therefore the input signal is amplified by $-C_1/C_B$ and is sampled by the capacitor C_a. The output voltage

$$V_{out}(n) = -\frac{C_1}{C_B} V_{in1}(n) \tag{13}$$

is obtained. At the same time, C_A is reset to zero. This makes this circuit work like sum-gain amplifier not like integrator.

During the period 2, the LHS plates of C_a and C_A are connected to the inverting terminal of the op-amp. Due to the offset voltage, this node can not function like the virtual ground. From the charge conservation, the charge stored in the C_A has to redistribute with C_A when the switches 2 are closed, because there is not charge transferred across C_o. The output voltage

$$V_{out}(n+\frac{1}{2}) = \frac{C_a}{C_A} V_{out}(n) + (1+\frac{C_a}{C_A}) V_{os} \tag{14}$$

can be derived. Combining the above two equations,

$$V_{out}(n+\frac{1}{2}) = \frac{-C_1 C_a}{C_A C_B} V_{in}(n) + (1+\frac{C_a}{C_A}) V_{os} \tag{15}$$

is obtained. The effective offset voltage is approximately reduced by the ratio of C_1/C_A when compared with the circuit without GOC. In the other words, dynamic range is also improved by that ratio. The dynamic range can be further improved by using the other circuit topologies like three-phase clocking scheme. But the chip layout will become more complicated and high-speed op-amp is also required. For the extremely low-gain case (gain $\ll$ 1), this GOC SGA is not suitable because the effective voltage V_{os} can not be reduced significantly. Other GOC SGA circuits should be designed.

The glitching problem may happen during the non-overlapping period if high-speed op-amps are used. This can be easily eliminated by connecting one additional capacitor C_m between the op-amp output and RHS plates of the capacitors C_B and C_a.

Acknowledgements

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